AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated below. The language being added is underlined ("__") and the language being deleted contains either a strikethrough ("~~~") or is enclosed by double brackets ("[[ ]]").

LISTING OF CLAIMS

1-34. (Canceled).

35. (Currently Amended) A method for preventing a DC flow condition caused by a transmit signal, comprising:

~~monitoring a data signal~~ determining whether a data signal exhibits a change in value;

generating a first signal in response to determining that the data signal does not exhibit a change in value ~~in response to a data signal condition~~ to prevent the DC flow condition;

monitoring a clock signal; and

generating a second signal in response to a clock signal condition to prevent the DC flow condition.

36. (Original) The method of claim 35, wherein the data signal is provided by a delta-sigma modulator.

37. (Original) The method of claim 35, wherein the step of monitoring a data

signal is performed with a digital comparator.

38. (Original) The method of claim 35, wherein the first signal is a power down signal.

39. (Canceled)

40. (Original) The method of claim 39, wherein the power down signal is generated by an asynchronous counter that reaches a maximum value.

41. (Original) The method of claim 35, wherein the second signal is a reset signal.

42. (Original) The method of claim 41, wherein the reset signal is generated in response to a clock signal having a frequency that fails to exceed a predetermined minimum value.

43. (Original) The method of claim 42, wherein the reset signal is generated by a monostable circuit.

44. (New) A method comprising:

monitoring a data signal to determine whether a data signal condition exists, wherein a data signal condition exists if the data signal maintains a present data level beyond a predetermined limit;

generating a power down signal in response to the data signal condition to prevent a DC flow condition;

monitoring a clock signal; and

generating a reset signal in response to a clock signal condition to prevent the DC flow condition.

45. (New) The method of claim 44, wherein the data signal is provided by a delta-sigma modulator.

46. (Original) The method of claim 41, wherein a clock signal condition exists if the clock signal has a frequency that fails to exceed a predetermined minimum value.

47. (New) The method of claim 44, wherein monitoring a data signal comprises:

initializing an asynchronous counter;

updating the asynchronous counter when the data level is maintained for more than one clock cycle;

resetting the asynchronous counter when the data level is not maintained for more than one clock cycle; and

determining whether the asynchronous counter exceeds the predetermined limit.

48. (New) The method of claim 44, wherein generating a reset signal comprises generating the reset signal using a monostable circuit.

49. (New) A method comprising:

monitoring a data signal;

generating a power down signal if the data signal maintains a present data level for a predetermined number of clock cycles;

monitoring for an anomalous clock signal comprising a clock signal with a frequency that fails to exceed a predetermined minimum value; and

generating a reset signal if an anomalous clock signal exists.

50. (New) The method of claim 49, wherein monitoring for an anomalous clock signal comprises monitoring how long the clock signal remains high and low.

51. (New) The method of claim 50, further comprising monitoring whether the clock signal remains high or low beyond a predetermined limit of time.

52. (New) The method of claim 49, wherein generating a reset signal comprises generating the reset signal using a monostable circuit.

53. (New) The method of claim 49, wherein monitoring a data signal comprises monitoring a data signal from a delta-sigma modulator.